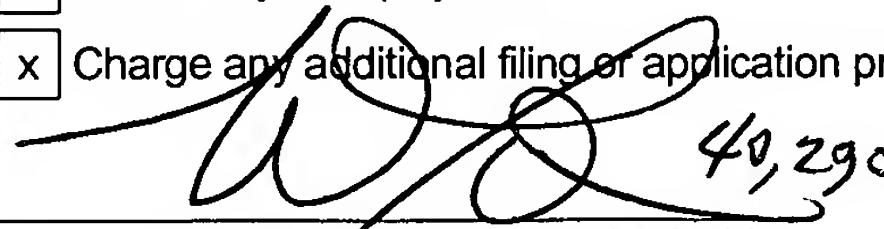


JPW



AMENDMENT TRANSMITTAL LETTER				Docket No. SON-2810	
Application No. 10/647,217-Conf. #1901		Filing Date August 26, 2003		Examiner D. B. Gandhi	
				Art Unit 2117	
Applicant(s): Yoshitaka Kayukawa et al.					
Invention: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME					
TO THE COMMISSIONER FOR PATENTS					
Transmitted herewith is an amendment in the above-identified application.					
The fee has been calculated and is transmitted as shown below.					
CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	19	- 23 =	0	x 50.00	0.00
Independent Claims	3	- 7 =	0	x 210.00	0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00
<input checked="" type="checkbox"/> Large Entity <input type="checkbox"/> Small Entity					
<input checked="" type="checkbox"/> No additional fee is required for this amendment.					
<input type="checkbox"/> Please charge Deposit Account No. _____ in the amount of \$ _____ A duplicate copy of this sheet is enclosed.					
<input type="checkbox"/> A check in the amount of \$ _____ to cover the filing fee is enclosed.					
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.					
<input checked="" type="checkbox"/> The Director is hereby authorized to charge and credit Deposit Account No. <u>18-0013</u> as described below. A duplicate copy of this sheet is enclosed.					
<input checked="" type="checkbox"/> Credit any overpayment.					
<input checked="" type="checkbox"/> Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.					
 40,290				Dated: <u>August 6, 2008</u>	
Ronald P. Kananen / Christopher M. Tobin Attorney/Agent Reg. No.: 24,104 / 40, 290					
RADER, FISHMAN & GRAUER PLLC 1233 20th Street, N.W. Suite 501 Washington, DC 20036 (202) 955-3750					



Docket No.: SON-2810
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yoshitaka Kayukawa et al.

Application No.: 10/647,217

Confirmation No.: 1901

Filed: August 26, 2003

Art Unit: 2117

For: SEMICONDUCTOR INTEGRATED CIRCUIT
AND METHOD FOR TESTING SAME

Examiner: D. B. Gandhi

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated May 28, 2008, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.